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10/693,788	10/24/2003	Toshimitsu Watanabe	16869P-095600US	2331

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EXAMINER	
PERVAN, MICHAEL	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/27/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/693,788	WATANABE ET AL.	
	Examiner	Art Unit	
	Michael Pervan	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/24/03, 6/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 9 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In regards to claim 9, the equation for determining C_i is not supported by the specification. Even though page 8, paragraph 26 refers to the equation for determining C_i, the equation only works for i = 1 and therefore it is unclear from the applicant's disclosure as to how this correction equation is implemented.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki et al (US 2002/0089473).

In regards to claim 1, Yamazaki discloses (Figures 1 and 3) a display unit comprising: a plurality of electron emission devices (11-14, 21-24) arranged in a matrix format (paragraph 28, lines 3-7); a plurality of scan lines (106) arranged in a row direction and connected to the plurality of electron emission devices (paragraph 29, lines 8-11 and paragraph 35; a select voltage pulse is applied to each line (row) sequentially to allow for emission of light, therefore there are a plurality of scan lines attached to electron emission devices (Surface Conduction Electron-emitting Devices, SCEs)); a plurality of data lines (105) arranged in a column direction and connected to the plurality of electron emission devices (paragraph 29, lines 3-8; column lines that have voltage pulse widths proportional to luminance data, electron emission requirement data, applied to them, therefore they are a plurality of data lines arranged in a column direction and connected to election-emission devices (SCEs)); a scan driver (106) for supplying a selection signal for selecting a line of electron emission devices to the scan lines sequentially in the column direction (paragraph 29, lines 8-11); a data driver (105) for supplying to each of the plurality of data lines a video-signal-based drive signal for driving the electron emission devices (paragraph 29, lines 3-8; column lines that have voltage pulse widths (video-signal-based drive signal), proportional to luminance data (electron emission requirement data) applied to them); and a signal corrector circuit (108) for correcting the drive signals to be supplied to the plurality of data lines in accordance with the video signal (paragraph 42; image signal (drive signal) from signal processing unit is corrected by adding a correction value to it, which would then generate an image signal with corrected luminance data).

In regards to claim 2, Yamazaki discloses the display unit according to claim 1 wherein the signal correction circuit (108) provides corrections, which vary with the position of the plurality of electron emission devices in the row direction (paragraph 54; correction is made due to voltage drops, since the voltage drops can vary for each device in a row, the correction also varies for each device in a row, therefore the correction varies by position).

In regards to claim 3, Yamazaki discloses the display unit according to claim 1 wherein an electrical current flows to each electron emission device in accordance with the potential difference between a selection signal and drive signal supplied to a plurality of electron emission devices in the selected line (paragraphs 43-53; drive current flows from the data lines to the electron emission devices (11-14) via the selected scan (row) line), and the correction values are determined so as to compensate for a voltage decrease in the row direction of each of the plurality of electron emission devices that is determined by the value of the current and the wiring resistance of the scan lines at various positions of a plurality of electron emission devices arranged in the row direction (paragraph 54; drive voltages are applied to all devices in a scan (row) line and due to voltage drops are compensated for to correct luminance data).

In regards to claim 4, Yamazaki discloses a display unit comprising: a display panel including scan lines (106) to which a selection signal is supplied for selecting a line of a plurality of electron emission devices arranged in a matrix format (paragraph 29, lines 8-11 and paragraph 35; a select voltage pulse is applied to each line

sequentially to allow for emission of light) and data lines (105) to which a video-signal-based drive signal is supplied for driving the plurality of electron emission devices (paragraph 29, lines 3-8; column lines that have voltage pulse widths (video-signal-based drive signal), proportional to luminance data (electron emission requirement data) applied to them); and a signal corrector circuit (108), wherein a current according to a potential difference between the selection signal and the drive signal flows to a plurality of electron emission devices in the selected line via scan lines connected to a plurality of electron emission devices in the selected line so that the electron emission devices emit electrons in accordance with the current (paragraphs 43-53; drive current flows from the data lines to the electron emission devices (11-14) via the selected scan (row) line and causes the device to emit electrons); and wherein the signal corrector circuit corrects each of the drive signals to be supplied to a plurality of electron emission devices in the selected line in accordance with the video signal in order to compensate for a voltage decrease that arises when the current flows to scan lines connected to a plurality of electron emission devices in the selected line (paragraph 54; drive voltages are applied to all devices in a scan (row) line and due to voltage drops are compensated for to correct luminance data).

In regards to claim 5, Yamazaki discloses a display unit comprising: a plurality of scan lines (106) extending in a row direction (paragraph 29, lines 8-11); a plurality of data lines (105) extending in a column direction (paragraph 29, lines 3-8); an electron emission device (11-14, 21-24) positioned at intersections of the plurality of scan lines and the plurality of data lines (Figure 3 and paragraph 28, lines 4-7; electron emission

devices (SCEs) of Figure 3 (11-14, 21-24) are at intersections of columns (data lines) and rows (scan lines)); a scan driver (106) for supplying a selection signal to select a line of the electron emission device to the plurality of scan lines sequentially in the column direction (paragraph 29, lines 8-11); a data driver (105) for supplying to each of the plurality of data lines a video-signal-based drive signal for driving the electron emission devices (paragraph 29, lines 3-8; column lines that have voltage pulse widths (video-signal-based drive signal), proportional to luminance data (electron emission requirement data) applied to them); and a signal corrector circuit (108) for individually correcting the drive signals to be supplied respectively to the plurality of electron emission devices (paragraphs 42 and 54; the correction quantity calculating unit compensates for a voltage drop of the drive voltage of the devices and does so for each device individually), wherein the signal corrector circuit corrects each of the drive signals by adding to the video signal correction values appropriate for a plurality of electron emission devices arranged in the row direction, so that each of the correction values varies with the magnitude of the video signal (paragraphs 42 and 54; each voltage drop is different for each device and depends on the drive voltage (video signal) applied, therefore each correction value, that is added, will be different and will depend on the drive voltage (video signal)).

In regards to claim 6, Yamazaki discloses the display unit according to claim 5 wherein the scan driver (106) is connected to one end of the scan lines so that the correction values increase with an increase in the distance between electron emission devices connected to the scan lines and the scan driver while the video signal remains

constant (paragraphs 50 and 54; since the voltage drop increases the further you are from the scan driver, the correction value increases, since it is based off the voltage drop).

In regards to claim 7, Yamazaki discloses the display unit according to claim 5 wherein the correction values are determined in accordance with the magnitude of voltage decrease at each position of a plurality of electron emission devices connected to the scan lines (paragraph 54).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 8 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki.

In regards to claim 8, Yamazaki discloses a display unit, comprising: a display panel in which m x n electron emission devices (11-14, 21-24) are arranged in a matrix format and positioned at the intersections of m scan lines (106) and n data lines (105), and phosphors (paragraph 28, lines 7-9) are positioned opposite the electron emission devices; a data driver (105) for sequentially supplying a column of video-signal-based drive signal to the n data lines (paragraph 29, lines 3-8; luminance data (video-signal-based drive signal) is applied to the columns lines (data lines)); a scan driver (106) for adding a selection signal for selecting a line of the electron emission devices to the m

scan lines sequentially in the column direction (paragraph 29, lines 8-11; a select voltage pulse (selection signal) is applied sequentially to the rows (scan lines)).

Yamazaki does not a signal corrector circuit for compensating for a voltage increase caused by the value Ii (i = 1 to n) of a current, which flows from each of n column wiring lines to the scan wiring for the selected line, when the scan driver selects a line.

Yamazaki discloses a signal corrector circuit (108) for compensating for a voltage decrease caused by the value Ii (i = 1 to n) of a current, which flows from each of n column wiring lines to the scan wiring for the selected line, when the scan driver selects a line (paragraphs 44-54; when a row (scan line) is selected current flows from the column drivers to the row drivers and a voltage drop is calculated from that current. Then a correction is calculated for each voltage drop to correct for luminance drops due to voltage drops).

This is viewed by the examiner to be a difference, but yet an obvious difference. Since, it would be obvious to compensate for a voltage decrease by increasing the voltage and to compensate for a voltage increase by decreasing the voltage.

In regards to claim 14, Yamazaki discloses (Figure 1) a display unit comprising: a display panel (107) in which a plurality of scan lines (106) extending in the row direction are arranged in the column direction, a plurality of data lines (105) extending in the column direction are arranged in the row direction, and a plurality of electron emission devices (11-14, 21-24) are mounted respectively at intersections of the plurality of scan lines and the plurality of data lines; a scan driver (106) that is connected to the plurality

of scan lines to supply a selection signal for selecting a line of the plurality of electron emission devices to the plurality of scan lines sequentially in the column direction (paragraph 29, lines 8-11); and a data driver (105) for supplying a video-signal-based drive signal for driving the electron emission devices to each of the plurality of scan lines (paragraph 29, lines 3-8; column lines that have voltage pulse widths (video-signal-based drive signal), proportional to luminance data (electron emission requirement data) applied to them).

Yamazaki does not disclose a white window pattern is displayed in a predetermined area within a totally black area, the level of the drive signal for a plurality of electron emission devices corresponding to the black area becomes constant, and the drive signal for a plurality of electron emission devices corresponding to the area of the white window pattern is corrected so that the drive signal increases gradually or stepwise as the distance to the scan driver increases in the row direction.

This, however, is viewed by the examiner to be an obvious difference. Since, on pixels would be considered to be white and off pixels would be considered to be black.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Suzuki et al (US 5,734,361).

In regards to claim 11, Yamazaki does not disclose the display unit according to claim 8 wherein the signal corrector circuit corrects the video data to be supplied to a data drive circuit for driving the video signal, positions the scan driver toward column n, and provides cumulative additive correction by multiplying the video signal amplitude Di of the i-th column by a predetermined coefficient.

Suzuki discloses the display unit according to claim 8 wherein the signal corrector circuit corrects the video data to be supplied to a data drive circuit for driving the video signal, positions the scan driver toward column n, and provides cumulative additive correction by multiplying the video signal amplitude Di of the i-th column by a predetermined coefficient (Figures 9a-9c and col. 12, lines 6-18; predetermined coefficients are shown in Figure 9c and are multiplied by the luminance signals in order to correct the luminance).

It would have been obvious at the time of invention to modify Yamazaki with the teachings of Suzuki, correct luminance levels in image signal, by replacing correction unit and adder of Yamazaki with totalizer, memory and multiplier of Suzuki because it would obtain a correct intensity for the display and prevent a deviation in display luminance of an image display device (col. 4, lines 45-49).

8. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Nakano (US 2003/0025717).

In regards to claim 12, Yamazaki discloses a display unit, comprising: a display panel in which a plurality of scan lines (106) extend in a row direction, a plurality of data (105) lines extend in a column direction, and a plurality of electron emission devices (11-14, 21-24) are mounted at intersections of the plurality of scan lines and the plurality of data lines; a scan driver (106) for supplying a selection signal for selecting a line of the plurality of electron emission devices to the plurality of scan lines sequentially in the column direction (paragraph 29, lines 8-11; a select voltage pulse (selection signal) is applied sequentially to the rows (scan lines)); a data driver (105) for supplying a video-

signal-based drive signal for driving the electron emission devices to each of the plurality of data lines (paragraph 29, lines 3-8; luminance data (video-signal-based drive signal) is applied to the columns lines (data lines)); an input section (100) for entering the video signal (paragraph 38; input terminal (input section) receives input of an image signal (video signal)) and a video signal processor circuit (101) for processing the video signal entered from the input section (paragraph 39; image signal processor (video signal processor) first samples (processes) the image signal (video signal) to fit the number of emitters and pixel information of the display); and a signal corrector circuit (108) for correcting a digital video signal received by the interface section and supplying the corrected signal to the data driver (paragraph 42; the correction value is added to the image signal from the image signal processor), wherein the signal corrector circuit corrects the drive signals to be supplied to a plurality of electron emission devices by adding correction values appropriate for the plurality of electron emission devices arranged in the row direction after calculating the correction values in accordance with the digital video signal (paragraphs 42 and 54; correction quantity is added to the image signal and the correction quantity depends and the drive voltage and voltage drop of each device).

Yamazaki does not disclose an interface section for transmitting/receiving the video signal output from the video signal processor circuit in digital form.

Nakano discloses (Figure 1) an interface section for transmitting/receiving (105, 206) the video signal output from the video signal processor circuit (103) in digital form

(paragraph 46, lines 19-25 and paragraph 49, lines 4-11; on the controller is a transmitter that sends image signals to the receiver on the display unit).

It would have been obvious at the time of invention to modify Yamazaki by incorporating Nakano, image signals are sent between a controller and display unit via a digital interface transmitter/receiver pair, because it would prevent a decline in image quality and make it possible to adjust the image quality of a displayed image (paragraph 4, lines 6-8).

In regards to claim 13, Yamazaki does not disclose the display unit according to claim 12 wherein the display panel, the scan driver, and the data driver constitute a display module; wherein a receiver of the interface section is positioned toward the display module; and wherein a transmitter of the interface section transmits a video signal from the video processor circuit to the receiver in digital form.

Nakano discloses (Figure 1) the display unit according to claim 12 wherein the display panel (202), the scan driver (203), and the data driver (204) constitute a display module; wherein a receiver (206) of the interface section is positioned toward the display module (paragraph 49, lines 12-19); and wherein a transmitter (105) of the interface section transmits a video signal from the video processor circuit to the receiver in digital form (paragraph 46, lines 19-23).

It would have been obvious at the time of invention to modify Yamazaki by incorporating Nakano, image signals are sent between a controller and display unit via a digital interface transmitter/receiver pair, because it would prevent a decline in image

quality and make it possible to adjust the image quality of a displayed image (paragraph 4, lines 6-8).

Response to Arguments

9. Applicant's arguments filed October 13, 2006 have been fully considered but they are not persuasive.

In regards to claim 9, Applicant (on page 8 or argument) argues that the equation is conventional mathematical notation of a very straightforward equation that relies on previous values. Examiner respectfully disagrees.

The example shown in Fig. 5 and described in the specification derives an equation different than the one claimed. The equation based on Fig. 5 and described in the specification is similar to the equation claimed, except that the summation should go from j=i to n. This will allow the summation to become smaller as the values of i become larger. Namely, when i=0 C_0=0 + (k times (D_0 + D_1 + D_2 + D_3 + D_4 + D_5 + D_6 + D_7 + D_8)) where (k times (D_0 + D_1 + D_2 + D_3 + D_4 + D_5 + D_6 + D_7 + D_8)) = B_8 based on the Fig. 5 and the description in the specification. For i=1 C_1=C_0 + (k times (D_1 + D_2 + D_3 + D_4 + D_5 + D_6 + D_7 + D_8)) where (k times (D_1 + D_2 + D_3 + D_4 + D_5 + D_6 + D_7 + D_8)) = B_7. However, in the current equation the summation is always equal to B_7, because it is always in the range from 1 to 8, so C_0 = 0 + B_7, C_1 = B_7 + B_7, so on and so forth. Therefore the equation as claimed is not supported by the specification.

In regards to claims 1, 4, 5, 8 and 12, Applicant (on page 9 of argument) argues that Yamazaki does not teach or even suggest the recited "signal correction circuit for correcting each of the drive signals to be supplied to the plurality of data lines, wherein

the signal correction circuit corrects the drive signals using a cumulative value of the video data corresponding to said drive signals." Examiner respectfully disagrees.

The applicant states in the line previous that "Yamazaki discloses correcting drive signals to compensate for voltage drop caused by wiring resistance", but then goes on to say that Yamazaki does not teach a signal correction circuit. This argument is circular and does not make any sense.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The Prior art (Hansen et al US 2003/0201954) is deemed relevant since it discusses image correction system. The Prior art (Moon US 2003/0210211) is deemed relevant since it discusses luminance compensation and correction that varies with the position of each cell.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Pervan whose telephone number is (571) 272-0910. The examiner can normally be reached on Monday - Friday between 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MVP
Dec 12, 2006

AMR A. AWAD
SUPERVISORY PATENT EXAMINER